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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,863	01/16/2004	Robert B. Staszewski	TI-35773	6568

23494 7590 12/26/2008
TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
12/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/758,863	STASZEWSKI ET AL.	
	Examiner	Art Unit	
	LEON FLORES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,11-43 and 45-54* is/are rejected.

7)☒ Claim(s) *10 and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 9/4/2008 have been fully considered but they are not persuasive.

Response to Remarks

Applicant asserts that *"a method for testing a radio frequency (RF) circuit" recited in the preamble is not taught or even suggested in Staszewski".*

2. The examiner respectfully disagrees. In response to applicant's arguments, the recitation "testing" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Furthermore, a preamble that recites the use or purpose of the claimed invention generally does not limit the claims. See Catalina, 62 USPQ2d at 1785.

Applicant further asserts that *"the step of"observing a signal from the RF circuit" is not taught in Staszewski. Due to the lack of testing there, there is no motivation of doing so. The "signal", equated by Examiner to PHE in Fig. 4a is not suggested to be observed for the purpose of testing. The PHE signal is only fed to the gain circuit 70 as part of a normal ADPLL operation, which has nothing to do with testing. No other*

connections are shown, especially to the "outside of the RF circuit"".

The examiner respectfully disagrees. The reference of Staszewski does teach observing a signal "PHE" from the RF circuit. (See fig. 4a) Furthermore, applicant does teach, in his disclosure, that the signal being observed is, in fact, the error signal generated within a PLL.

Applicant further asserts that *"the limitation of"wherein the signal has a high degree of correlation with an RF output of the RF circuit" is not taught or suggested in Staszewski. At the time of the reference patent publication, the ADPLL idea was still quite new and it would not have been known by one of average skill in the art that the PHE signal has a high degree of correlation with "an RF output", such as output of the PA circuit".*

The examiner respectfully disagrees. One skilled in the art would know that by filtering out frequencies components (not desired) which are above the cut off frequency of the loop filter, a high degree of correlation between the phase error (desired frequencies) and the RF output can be achieved. This is notoriously well known in ADPLLs.

Applicant further asserts that *"Staszewski fails to teach or suggest, a method for testin~ a radio frequency (RF) circuit comprising: "observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit, wherein the signal has a high degree of correlation with an RF output of the RF circuit, and wherein the observing occurs outside of the RF circuit", "manipulating the signal outside of the RF circuit" and "producing a metric for the test outside of the RF circuit*

based on results from the manipulating", as required by Claim 1".

The examiner agrees. However, the examiner did not rely solely in the reference of Staszewski to reject claim 1. The examiner used the combination of Staszewski and Wong to reject claim 1.

Applicant further asserts that *"Moreover, even had the Examiner considered all of the words of Claim 1, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703,705, 223 USPQ 1257, 1258 (Fed. Cir. 1988))".*

The examiner respectfully disagrees. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both the references of Staszewski and Wong deal with PLLs.

Applicant further asserts that *"Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Gordon, 733 F.2d at 902, 221 USPQ at 1127. Moreover, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Fell, 774 F.2d 1132, 1138,227 USPQ 543,547 (Fed.Cir.1985)".*

The examiner respectfully disagrees. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant further asserts that *"Staszewski does not teach "wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation" limitation, as required by Claim 41".*

The examiner agrees. However, the examiner did not use the reference of Staszewski to reject this limitation. The examiner, in the other hand, used the reference of Wong to reject this limitation.

Applicant further asserts that *"to copy from the previous amendment: detector containing circuitry to compute a difference between the reference phase and a variable phase .... ". Wong only teaches UP/DOWN phase direction information, which is not the phase error estimation signal. There is no magnitude information, only the direction.">>. As such, Examiner's determination of the teaching of Wong is erroneous".*

The examiner respectfully disagrees. The reference of Wong does teach that this signal is the phase error. (See fig. 2 & col. 2, lines 50-57 "phase error information") However, taking the contrary, applicant, at any point, claims that the signal must show magnitude information.

Applicant further asserts that *"Moreover, even had the Examiner considered all of the words of Claim 41, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703,705, 223 USPQ 1257, 1258*

(Fed. Cir. 1988)".

The examiner respectfully disagrees. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both the references of Staszewski and Wong deal with PLLs.

Applicant further asserts that *"Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Gordon, 733 F.2d at 902, 221 USPQ at 1127. Moreover, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543,547 (Fed.Cir.1985)".*

The examiner respectfully disagrees. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references.

See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant further asserts that *"Moreover, Applicants disagree with Examiner's contention that one skilled in the art "would know that if the loop filter is designed in such as way (adjusting filter's parameters) so that the frequency of the error signal is within the cutoff frequency of the loop filter, then a high degree of correlation can be achieved between the error signal and the output signal". Applicants respectfully request Examiner to provide evidence from the prior art supporting his assertion or withdraw the determination. Furthermore, when a high degree of correlation is achieved the transfer function will be flat within a specific frequency range". At the time of the instant application, the knowledge that the digital PHE signal was highly correlated with the RF output phase, and their transfer function was flat, was not obvious".*

The examiner respectfully disagrees. One skilled in the art would know that by filtering out frequencies components (frequency components not desired) which are above the cut off frequency of the loop filter, a high degree of correlation between the phase error (desired frequencies) and the RF output can be achieved. This is notoriously well known in ADPLLs.

Applicant further asserts that *"First, the circuit disclosed in Wong's Fig. 2 is not an "all digital circuit" (as required by the parent Claim 6), but rather a "very high frequency phase locked loop" with a number of analog components and signals. The Digital Loop Filter 14 in Wong does not operate on a digital phase error signal but analog UP/DOWN pulses in which the information is contained in the pulse widths. The*

analog nature of circuit 14 is described in col. 3 as "The loop filter 14 of the DPLL includes a scaler circuit, an integrator circuit, and a summing circuit emulating a 1-pole/l-zero digital loop filter". Hence, Examiner's combination of Staszewski and Wong to obviate Claim 8 is improper and must be withdrawn".

The examiner respectfully disagrees. The reference of Wong does teach that the PLL is a Digital Phase Lock Loop. (See col. 3, line 14, col. 4, lines 36-37 "DPLL")

Applicant further asserts that *"Claim 24 further defines the method of claim 1, wherein the RF circuit contains an all-digital phase-locked loop, and the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth. Claim 24 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, the text in Wong cited by Examiner does not teach "the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth", as required by Claim 24. The text only mentions setting of various programmability modes, NOT bandwidths: "The loop filter also includes a loop configuration circuit which in response to the digital tester 4 programs and via the LCP 24 configures the loop type of the DUT 2. The DPLL, for example, provides for different types of loop configurations in a test mode (8 different combinations of close loop, open loop, and enable/disable proportional/integral paths) as shown in Table 1 ." As such, any combination of Staszewski and Wong fails to teach or suggest all of the elements of Claim 24. The 35 U.S.C. 103 (a) rejection is erroneous and must be withdrawn"*.

The examiner respectfully disagrees. The reference of Wong does teach "the loop filter also includes a loop configuration circuit for configuring the loop type of the

DUT. (See col. 3, lines 19-26 & table 1) Furthermore, one skilled in the art would know that loop configuration is dependent on loop bandwidth. Furthermore, the loop bandwidth is dependent on what type of loop configuration the PLL will be operating.

Applicant further asserts that *"Claim 26 further defines the method of claim 25, wherein the setting, observing, and manipulating is repeated for several different all-digital phase-locked loop bandwidths, and wherein the producing comprises subtracting the calculated mean square errors for the several different all-digital phase-lock loop bandwidths. Claim 26 is allowable for the same reasons set forth above in support of the allowance of Claim 25. Moreover, Wong does not teach selecting different loop bandwidths. The loop configuration in the cited text selects, for example, between open loop, closed loop, etc, modes, which have nothing to do with selecting loop bandwidths. As such, Wong does not teach their repeated application of "setting, observing, and manipulating" "for several different all-digital phase-locked loop bandwidths", as required by Claim 26. The statement by Examiner "Furthermore, one skilled in the art would know that the loop bandwidth varies depending if the PLL is in either acquisition or tracking mode" attempts to suggest obviousness but is irrelevant here since the loop bandwidth change in the present invention has nothing to do with PLL acquisition or tracking mode, but pertains to the testing method itself. As such, any combination of Staszewski and Wong fails to teach or suggest all of the elements of Claim 26. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn".*

The examiner respectfully disagrees. The reference of Wong does teach "the loop filter also includes a loop configuration circuit for configuring the loop type of the

DUT. (See col. 3, lines 19-26 & table 1) Furthermore, one skilled in the art would know that loop configuration is dependent on loop bandwidth. Furthermore, the loop bandwidth is dependent on what type of loop configuration the PLL will be operating.

Applicant further asserts that *"Claim 15 further defines the method of claim 14, wherein the phase error trajectory is good when the change in the signal is less than a specified threshold. Claim 15 is allowable for the same reasons set forth above in support of the allowance of Claim 14. Moreover, none of the references pertain to the "test ... for phase error trajectory". Further, the references, alone or in combination, do not teach the limitation of"wherein the manipulation comprises measuring a change in the signal". Examiner's statement, "The error signal is further compared with a threshold in order to determine if a coarse or fine adjustment is needed", is irrelevant as it does not pertain to "change in the signal" and testing in general. As such, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 15. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn".*

The examiner respectfully disagrees. One skilled in the art would know that the phase error is the main signal of interest within a PLL. When the phase error is must be kept minimized in order to maintain synchronization.

Applicant further asserts that *"Claim 16 further defines the method of claim 14, wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. Claim 16 is allowable for the same reasons set forth above in support of the allowance of Claim 14. Moreover, none of the references teach or suggest "measuring a peak, a variance, or a rate of change in the*

signal". The circuits are not designed for and are not capable of these measurements. The Examiner's cited text "Preferably, an error signal 104 compares unfavorably when it exceeds the coarse threshold -- when the coarse threshold signal is logic high" (col. 5, lines 37-39) has noting to do with the limitation of"comparing a value of the signal over several samples". As such, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 16. The 35 U.S.C. 103 (a) rejection is erroneous and must be withdrawn".

The examiner respectfully disagrees. The error signal is compared to a threshold in order to determine if synchronization is achieved and/or maintained. This is notoriously well known in PLLs.

Applicant further asserts that *"Claim 17 further defines the method of claim 1, wherein the test is for frequency lock and the signal is the output of a phase detector, and wherein the manipulation comprises comparing a value of the signal over several samples. Claim 17 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, Examiner's cited text "Preferably, an error signal 104 compares unfavorably when it exceeds the coarse threshold -- when the coarse threshold signal is logic high" (col. 5, lines 37-39) has noting to do with the above limitation. As such, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 17. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn".*

The examiner respectfully disagrees. The error signal is compared to a threshold in order to determine if synchronization is achieved and/or maintained. This is

notoriously well known in PLLs.

Applicant further asserts that *"Claim 19 further defines the method of claim 17, wherein the samples are taken at different times. Claim 19 is allowable for the same reasons set forth above in support of the allowance of Claim 17. Moreover, Examiner's cited text "Preferably, an error signal 104 compares unfavorably when it exceeds the coarse threshold -- when the coarse threshold signal is logic high" (col. 5, lines 37-39) has noting to do with the above limitation. Further, and contrary to Examiner's determination, Girardeau does NOT teach the limitation of "wherein the samples are taken at different times". As such, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 19. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn".*

The examiner respectfully disagrees. At one time the error is compared to a coarse threshold. At another (later) time the error signal is compared to a fine threshold. This is mainly done in order to determine if synchronization has been achieved/maintained. This is notoriously well known in PLLs.

Applicant further asserts that *"Claim 20 further defines the method of claim 1, wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter, and wherein the manipulation comprises comparing the signal with a specified range. Claim 20 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, the references, alone or in combination, do not teach the limitation of"wherein ... the signal is an output of an integral accumulator of a loop filter". The text cited by Examiner "The DPLL 10*

determines a correct divisor upon startup, corrects for frequency drifts, 20 and is able to operate in noisy conditions" (col. 5, lines 19-21) is irrelevant and does not mention the "integral accumulator of the loop filter". Furthermore, the references fail to teach "wherein the manipulation comprises comparing the signal with a specified range". Comparing with a threshold is not equivalent with comparing with a specified range. In the event Examiner maintains this argument, Applicants respectfully request that Examiner provide evidence from the prior art supporting his determination. As such, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 20. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn".

The examiner respectfully disagrees. The reference of Girardeau does teach the signal is an output of an integral accumulator of a loop filter. (See fig. 1: 24 “loop filter”. Designs featuring accumulators in loop filters are well known in the art.) Furthermore, one skilled in the art would know that a threshold specifies a range.

Applicant further asserts that *“Moreover, Figure 4 in Ko does not show "a plurality of filters arranged in a parallel fashion", as suggested by Examiner. The cited text (col. 2, lines 45-52) describes the structure filters as n filters with the phase detector selecting one filter among the n filters. In addition, combining Ko into Girardeau would not work since the output of such a filer could not be connected to the oscillator 23”.*

The examiner respectfully disagrees. The reference of Ko does teach a plurality of filters arranged in a parallel fashion. (See fig. 4) Furthermore, In response to applicant's argument that “the combination of Ko into Girardeau would not work", the

test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Applicant further asserts that *"Kim's teaching of BIST is not applicable to the combination of Staszewski and Wong. Kim teaches the use of the traditional pulse-based phase detector and charge pump. It also requires the VCO divider. None of these circuits is used in Staszewski so Kim is not relevant here.*

The examiner respectfully disagrees. In response to applicant's argument that "the combination of Kim and Staszewski would not work", the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Applicant further asserts that *"Claim 10 further defines the method of claim 8, wherein the all-digital phase- lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter. Claim 10 is allowable for the same reasons set forth above in support of the allowance of Claim 8. Moreover, and contrary to Examiner's determination, there is no teachings in Mathe that "the signal is an output of an infinite impulse response filter coupled to the*

output of a loop filter", as required by Claim 10. The text cited by Examiner in Mathe, "Loop filter 108 can also be implemented as a digital filter such as an infinite impulse response (IIR) filter" (col. 5, lines 32-37), teaches only implementation of one and only one filter, not one coupled to another. As such, any combination of Staszewski, Wong and Mathe fails to teach or suggest all of the elements of Claim 10. The, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn".

The examiner agrees. This rejection has been withdrawn.

Applicant further asserts that *"Claim 44 further defines the circuit of claim 43, wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof. Claim 44 is allowable for the same reasons set forth above in support of the allowance of Claim 43. Moreover, and contrary to Examiner's determination, there is no teaching in Mathe that "wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof", as required by Claim 44. The text cited by Examiner in Mathe, "Loop filter 108 can also be implemented as a digital filter such as an infinite impulse response (IIR) filter" (col. 5, lines 32-37), teaches only implementation of one and only one filter, not a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof. As such, any combination of Staszewski, Wong and Mathe fails to teach or suggest all of the element*s of Claim 44. The, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn".

The examiner agrees. This rejection has been withdrawn.

Applicant further asserts that *"Wong's system is engineered in such as way as to minimize the data rate accessible through the I/O controller. Hence, the phase detector 10 output is not accessible nor is the PEP 12 output - making them available (despite various technical difficulties) would not provide any substantial benefits. For the above reasons, Wong does not teach or suggest, "a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals." The interface in Wong is asynchronous and there is simply no motivation to re-engineer the entire architecture, which in itself is non-obvious to one of average skill in the art at the time of the invention, to allow synchronous signal controls of sufficient speed, as suggested by Examiner.*

The examiner respectfully disagrees. The reference of Wong does suggest a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals. (See fig. 1 & col. 1, lines 56-61 'digital tester" "keyboard")

Applicant further asserts that *"Moreover, Wong does not teach or suggest the limitation of"to provide a performance metric for the RF circuit", as further required by Claim 32. Wong teaches only testing and does not even suggest performance estimation. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn".*

The examiner respectfully disagrees. The reference of Wong does suggest provide a performance metric for the RF circuit. (See fig. 1 & col. 1, lines 56-61 & fig. 2 & col. 1, lines 45-48, 56-61, col. 2, lines 36-40, col. 4, lines 6-15)

Applicant further asserts that *"Claim 36 further defines the circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector. Claim 36 is allowable for the same reasons set forth above in support of the allowance of Claim 32. Furthermore, Examiner is not correct in asserting that the processor in Wong "is coupled to an output of a phase detector". The tester 4, equated by Examiner to the processor, is coupled only to LCP, FAP and PAP, with FAP being the closest to the output of the phase detector".*

The examiner respectfully disagrees. The reference of Wong does suggest a tester 4 coupled to the output of phase detector. (See fig. 2 & col. 3, lines 14-21 & col. 4, lines 6-16)

Applicant further asserts that *"Claim 38 further defines the circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector and a filtered output of a phase detector. Claim 38 is allowable for the same reasons set forth above in support of the allowance of Claim 32. Furthermore, Examiner is not correct in asserting that the processor in Wong "is coupled to an output of a phase detector". The tester 4, equated by Examiner to the processor, is coupled only to LCP, FAP and PAP, with FAP being the closest to the output of the phase detector. The phase detector 10 output contains information of the phase error, which is the phase difference between the Din and P_CLK inputs to the phase detector. FAP 26 register, on the other hand, contains "the frequency difference between Din and the local clock generated by the local crystal"*

(col. 4, lines 60-62) - this is definitely not the phase error. Hence, the tester 4 is not coupled to the phase detector. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn".

The examiner respectfully disagrees. The reference of Wong does suggest a tester 4 coupled to the output of phase detector.("which is the loop filter for setting the loop configuration") (See fig. 2 & col. 3, lines 14-21 & col. 4, lines 6-16 & col. 4, lines 50-55)

Applicant further asserts that *"The text cited by Examiner discusses only a "cost efficient comprehensive testing" at IC level and communication board level. It mentions "in field servicing (on-site)", which simply implies a lab environment and is different from "in field" testing. The specification of the instant application describes ([0048] of the publication) "in field testing" as "testing can usually be done without the use of expensive laboratory equipment", and "the testing can be performed while the electronic device is in the end-user's hands". The system in Wong with the external test equipment 4 in Fig. 2 is simply not capable of"in-field testing". Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn".*

The examiner respectfully disagrees. The reference of Wong does suggest in field. (See col. 4, lines 16-27 "network services")

Applicant further asserts that *"Examiner admits that Kim fails to teach or suggest, "reporting to a cellular service provider through a wireless medium when the BIST reports the parameter to be degraded beyond a limit" (Office communication page 31, lines 3-5). Examiner relies instead on Perez to provide this teaching. But even if,*

arguendo, Perez provides this teaching, Examiner misinterprets the remaining teaching of Kim. In actuality, Kim describes fault testing of a PLL, which is a narrow area well defined in the arts. To cite from Kim: "structural and defect-oriented testing" (Abstract), "defect-oriented testing" (col. 2, line 10). It does not teach performance testing associated with a cellular phone, nor does it even go beyond the PLL, which is merely a small building block of a cell phone. Specifically he does not teach "performing built-in self-test (BIST) on a parameter associated with the cellular phone", as required by Claim 48. Therefore, even if, arguendo, Perez teaches what Examiner proposes, the combination of Kim and Perez yet fails to teach or suggest, "performing built-in self-test (BIST) on a parameter associated with the cellular phone", as required by Claim 48. Accordingly, the 35 U.S.C. 103(a) rej ection of Claim 48 is improper and must be withdrawn".

The examiner respectfully disagrees. One skilled in the art would know that PLLs are inherent features in cellular phones. Therefore, the combination of Kim and Perez does suggest the teaching of performing built-in self-test (BIST) on a parameter associated with the cellular phone. (In Perez, see abstract, col. 5, line 26 – col. 6, line 15)

Applicant further asserts that *"Moreover, even had the Examiner considered all of the words of Claim 48, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The*

Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703,705,223 USPQ 1257, 1258 (Fed. Cir. 1988))".

The examiner respectfully disagrees. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both references deal with an inherent component, such as a PLL, within a cellular device.

Applicant finally asserts that *"although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Gordon, 733 F.2d at 902, 221 USPQ at 1127. Moreover, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so*

that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543,547 (Fed.Cir.1985)".

The examiner respectfully disagrees. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of *"wherein the all-digital phase-lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter"* must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims (1, 3, 5-8, 11, 13-14, 24-29, 31, 41-43) are rejected under 35 U.S.C.

103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) in view of Wong et al (hereinafter Wong) (US Patent 5,295,079) for the same reasons as set forth in the last office action.

Re claim 1, Staszewski discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit. (See fig. 4A: “PHE”)

But the reference of Staszewski fails to explicitly teach that wherein the signal has a high degree of correlation with an RF output of the RF circuit.

However, one skilled in the art would know that if the loop filter is designed in such as way (adjusting filter's parameters) so that the frequency of the error signal is within the cutoff frequency of the loop filter, then a high degree of correlation can be achieved between the error signal and the output signal.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, in the manner as claimed, for the benefit of achieving synchronization.

The reference of Staszewski discloses the limitations as claimed, except he fails to explicitly teach that wherein the observing occurs outside of the RF circuit; manipulating the signal outside of the RF circuit; and producing a metric for the test outside of the RF circuit based on results from the manipulating.

However, Wong does. The reference of Wong does teach "to enhance accuracy, the digital tester 4 averages several readings of FAP 26. Based on the average reading of FAP 26, the digital tester 4 calculates the expected output frequency (fm) of the PFC

16". (See col. 4, lines 59-65) By averaging several readings of FAP, the tester is somehow manipulating data from the PLL.

Furthermore, the reference of Wong also teaches “these digital signals are accessible through several on-chip (PLL) read/write ports allowing an external intelligent digital circuit (the tester) to compute the PLL dynamic performance" (See col. 1, lines 45-48), “providing a digital testing approach to measure RXC jitter” (See col. 4, lines 50-52), and this is done “by calculating the difference between the measured, PAP 28 readings and the predicted PAP 28 contents”, and these readings are illustrated in an oscilloscope. (See col. 5, lines 6-16 & fig. 4)

And finally, Wong also teaches a table which lists the various tests necessary to ensure the proper functioning of a typical PLL circuit. (See col. 6, lines 29-36 & Table 2) Please note that in table 2, a spectrum analyzer is used in order to test FCO clock spectral purity). One skilled in the art would know that the spectrum analyzer (signal analyzer) is capable of observing, manipulating, and generating performance metrics.

Taking the combined teachings of Staszewski and Wong as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, in the manner as claimed and as taught by Wong, for the benefit of optimizing the performance of the PLL.

Re claim 3, the combination of Staszewski and Wong further discloses that wherein the signal is a phase error signal. (In Staszewski, see fig. 4A: “PHE”)

Re claim 5, the combination of Staszewski and Wong fails to explicitly teach that

that wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest.

However, one skilled in the art would know that if the loop filter is designed in such as way (adjusting filter's parameters) so that the frequency of the error signal is within the cutoff frequency of the loop filter, then a high degree of correlation can be achieved between the error signal and the output signal. Furthermore, when a high degree of correlation is achieved the transfer function will be flat within a specific frequency range.)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

Re claim 6, the combination of Staszewski and Wong further discloses that wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit. (In Staszewski, see fig. 4A)

Re claim 7, the combination of Staszewski and Wong further discloses that wherein the signal is an output of a phase detector. (In Staszewski, see fig. 4A: “PHE” & 68)

Re claim 8, the combination of Staszewski and Wong further discloses that

wherein the signal has been filtered. (In Wong, see fig. 2: 14)

Re claim 11, the combination of Staszewski and Wong further discloses that wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output of the loop filter. (In Wong, see fig. 2: 14)

Re claim 13, the combination of Staszewski and Wong further discloses that wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output. (One skilled in the art would know that the frequency of the error signal, outputted from the phase comparator, is less than the RF frequency.)

Re claim 14, the combination of Staszewski and Wong fails to disclose that wherein the test is for phase error trajectory and the signal is the output of a phase detector, and wherein the manipulation comprises measuring a change in the signal.

However, the reference of Wong does teach measuring a change phase error outputted from the phase detector. (See fig. 2: 26 & 28 & figs. 3A, 4A, 4B, 4C)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

Re claim 24, the combination of Staszewski and Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop. (In Staszewski, see fig. 4A)

But the combination of Girardeau and Yamaguchi fails to explicitly teach that the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth.

However, the reference of Wong does teach a loop configuration circuit which in response to the digital tester programs and via the LCP configures the loop type of the Device under test "DUT". (See col. 3, lines 19-26 & table 1)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

Re claim 25, the combination of Staszewski and Wong fails to explicitly teach that wherein the test is for estimating phase noise power and the signal is an output of a phase detector, and wherein the manipulating comprises calculating a mean square error of the signal.

However, the reference of Wong does suggest calculating RXC jitter by phase meter. (See col. 4, line 41 - col. 5, line 16) Furthermore, one skilled in the art would know that the mean square error of the signal can be computed once the phase error is determined.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

Re claim 26, the combination of Staszewski and Wong fails to explicitly teach that wherein the setting, observing, and manipulating is repeated for several different all-digital phase-locked loop bandwidths, and wherein the producing comprises subtracting the calculated mean square errors for the several different all-digital phase-lock loop bandwidths.

However, the reference of Wong does suggest selecting loop configuration based on selected application, and minimizing the phase error signal in order to achieve frequency/phase lock. (See col. 3, lines 19-26) Furthermore, one skilled in the art would know that the loop bandwidth varies depending if the PLL is in either acquisition or tracking mode.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

Re claim 27, the combination of Staszewski and Wong further discloses that wherein the RF circuit is an all-digital frequency synthesizer. (In Staszewski, see fig. 4A)

Re claim 28, the combination of Staszewski and Wong further discloses that wherein the RF circuit is an all-digital transmitter. (In Staszewski, see paragraph 59)

Re claim 29, the combination of Staszewski and Wong further discloses that wherein the transmitter is used in a wireless communications network. (In Staszewski, see paragraph 59)

Re claim 31, the combination of Girardeau and Yamaguchi further discloses that wherein the testing comprises a functional test or a compliance test of the RF circuit. (In Wong, see col. 1, line 38 – col. 2, line 3)

Re claim 41, Staszewski discloses a circuit comprising: a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase (See fig. 4A: 62 & paragraph 44); a phase detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase (See fig. 4A: 68 & paragraph 44); a digitally-controlled oscillator (DCO) coupled to the phase detector (See fig. 4A: 74 & paragraph 44), a variable phase accumulator coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase. (See fig. 4A: 66 & paragraph 46)

But the reference of Staszewski fails to teach that wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation.

However, Wong does. The reference of Wong does teach "to enhance accuracy, the digital tester 4 averages several readings of FAP 26. Based on the average reading of FAP 26, the digital tester 4 calculates the expected output frequency (fm) of the PFC

16". (See col. 4, lines 59-65) By averaging several readings of FAP, the tester is somehow manipulating data from the PLL.

Furthermore, the reference of Wong also teaches “these digital signals are accessible through several on-chip (PLL) read/write ports allowing an external intelligent digital circuit (the tester) to compute the PLL dynamic performance" (See col. 1, lines 45-48), “providing a digital testing approach to measure RXC jitter” (See col. 4, lines 50-52), and this is done “by calculating the difference between the measured, PAP 28 readings and the predicted PAP 28 contents”, and these readings are illustrated in an oscilloscope. (See col. 5, lines 6-16 & fig. 4)

And finally, Wong also teaches a table which lists the various tests necessary to ensure the proper functioning of a typical PLL circuit. (See col. 6, lines 29-36 & Table 2) Please note that in table 2, a spectrum analyzer is used in order to test FCO clock spectral purity). One skilled in the art would know that the spectrum analyzer (signal analyzer) is capable of observing, manipulating, and generating performance metrics.

Taking the combined teachings of Staszewski and Wong as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, in the manner as claimed and as taught by Wong, for the benefit of optimizing the performance of the PLL.

Re claim 42, the combination of Staszewski and Wong further disclose a time-to-digital converter (TDC) coupled to the DCO and the phase detector, the TDC containing circuitry to compute a time difference between a reference clock and a variable clock.

(In Staszewski, see fig. 6 & paragraph 51)

Re claim 43, the combination of Staszewski and Wong fails to explicitly teach a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase.

However, the reference of Staszewski does teach a loop gain coupled to the phase detector and the DCO. (See fig. 4A: 70) One skilled in the art would know that the loop gain is a function of the loop filter and other parameters within the PLL.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

2. Claims (15-17, 19-21) are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Girardeau, Jr (hereinafter Girardeau) (US Patent 5,486,792) for the same reasons as set forth in the last office action.

Re claim 15, the combination of Staszewski and Wong fails to explicitly teach that wherein the phase error trajectory is good when the change in the signal is less than a specified threshold.

However, Girardeau does. (See fig. 2: error signal & col. 5, lines 37-39) Girardeau discloses a digital phase lock loop "DPLL" wherein an error signal is generated based on a comparison between a reference signal and a feedback signal. The error signal is further compared with a threshold in order to determine if a coarse or fine adjustment is needed.

Taking the combined teachings of Staszewski, Wong, and Girardeau as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, as modified by Wong, in the manner as claimed and as taught by Girardeau, for the benefit of optimizing the performance of the PLL.

Re claim 16, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 17, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the test is for frequency lock and the signal is the output of a phase detector (In Girardeau, see col. 2, lines 30-37 & col. 4, lines 65-67), and wherein the manipulation comprises comparing a value of the signal over several samples. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold. Furthermore, during tracking mode the PLL tries to keep the phase locked.)

Re claim 19, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the samples are taken at different times. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold. Furthermore, during tracking mode the PLL tries to keep the phase locked.)

Re claim 20, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter (In Girardeau, see col. 5, lines 19-21), and wherein the manipulation comprises comparing the signal with a specified range. (In Girardeau, see col. 2, lines 30-36. The error signal is being compared with the threshold.)

Re claim 21, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the frequency deviation is within acceptable limits when the signal is within the specified range. (In Girardeau, see col. 2, lines 30-36)

Re claim 22, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the manipulation further comprises comparing several samples of the signal. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold.)

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claims 1 & 41 above, and further in view of Ko (US Patent 5,982,832) for the same reasons as set forth in the last office action.

Re claim 45, the combination of Staszewski and Wong fails to disclose that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion.

However, Ko does. (See fig. 4 & col. 4, lines 18-25) Ko discloses a plurality of filters arranged in a parallel fashion.

Therefore, taking the combined teachings of Staszewski, Wong and Ko as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, as modified by Wong, in the manner as claimed and as taught by Ko, for the benefit of achieving phase compensation.

Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claims 1 & 41 above, and further in view of Cucchietti et al (hereinafter Cucchietti) (US Patent 4,819,080) for the same reasons as set forth in the last office action.

Re claim 46, the combination of Staszewski and Wong fails to disclose that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are

arranged in a cascaded fashion.

However, Cucchietti does. (See fig. 4: "BP" & col. 2, lines 45-52) Cucchietti discloses two cascaded filters located at the output of a phase detector.

Therefore, taking the combined teachings of Staszewski, Wong, and Cucchietti as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, as modified by Wong, in the manner as claimed and as taught by Cucchietti, for the benefit of achieving passing the desired frequencies and eliminating the non-desired frequencies.

1. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Kim et al (hereinafter Kim) (US Patent 6,885,700 B1) for the same reasons as set forth in the last office action.

Re claim 2, the combination of Staszewski and Wong fails to specifically disclose that wherein the testing is performed using built-in self-test (BIST) techniques.

However, Kim does. (See abstract & col. 1, lines 13-40) Kim discloses a charge-based frequency technique that performs structural and defect-oriented testing and uses existing blocks to save die area.

Taking the combined teachings of Staszewski, Wong, and Kim as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system of Staszewski, as modified by Wong, in the manner as claimed and as taught by Kim,

for the benefit of providing proper stimulus for the loop filter located inside the PLL.

Claims (9, 12, 30 & 47) are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claims 1 & 41 above, and further in view of Staszewski et al (hereinafter Staszewski I) (US Publication 2002/0094052 A1) for the same reasons as set forth in the last office action.

Re claim 9, the combination of Staszewski and Wong further disclose, that the signal is an output of an integral accumulator of a loop filter. (See col. 3, lines 14-15)

But the combination of Staszewski and Wong fails to teach that wherein the all-digital phase-lock loop is operating in a type-II mode.

However, Staszewski I does. (See paragraph 2)

Taking the combined teachings of Staszewski, Wong, and Staszewski I as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system Staszewski, as modified by Wong, in the manner as claimed, and as taught by Staszewski I, for the benefit of optimizing the PLL.

Re claim 12, the combination of Staszewski, Wong, and Staszewski I further disclose that wherein the signal is an output of a gain normalization block. (In Staszewski I, see fig. 5: “DCO Gain Normalization”)

Re claim 30, the combination of Staszewski, Wong, and Staszewski I further

discloses that wherein the wireless communications network is Bluetooth compliant. (In Staszewski I, see paragraph 32)

Re claim 47, Staszewski, Wong, and Staszewski I a gain normalization unit coupled to the phase detector and the DCO, the gain normalization unit to normalize the difference between the reference phase and the variable phase with respect to a gain in the DCO. (In Staszewski I, see fig. 5: "DCO Gain Normalization")

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Gustafson et al (hereinafter Gustafson) (US Patent 4,086,539) for the same reasons as set forth in the last office action.

Re claim 18, the combination of Staszewski and Wong fails to specifically disclose that wherein if a variance in the magnitude is less than a specified threshold, then the frequency has been locked.

However, Gustafson does. (See abstract & col. 1, lines 37-40) Gustafson discloses that phase lock loops produce favorable results in terms of phase-error variance in high frequency system and below threshold.

Taking the combined teachings of Staszewski, Wong, and Gustafson as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system Staszewski, as modified by Wong, in the manner as claimed, and as taught by

Gustafson, for the benefit of locking the frequency.

3. Claims (32-40) are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al (hereinafter Wong) (US Patent 5,295,079) for the same reasons as set forth in the last office action.

Re claim 32, Wong discloses a circuit comprising: a processor coupled to a radio frequency (RF) circuit. (See fig. 2)

But the reference of Wong fails to explicitly teach that the processor containing circuitry to manipulate digital signals from the RF circuit to provide a performance metric for the RF circuit; and a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals.

However, the reference of Wong does suggest that the teachings of digital tester (an intelligent digital controller) coupled to an input "keyboard" (See fig. 1: the input of element 4 & col. 1, lines 56-61), that performs tests, extract, and interpret data from the device under test (DUT). Furthermore, table 2 shows several of how to test some PLL dynamic performance parameters. (See fig. 2: 4 & col. 1, lines 45-48, 56-61, col. 2, lines 36-40, col. 4, lines 6-15)

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of testing some PLL dynamic performance parameters. (See col. 6, lines 29-31)

Re claim 33, the reference of Wong fails to disclose a latch coupled to the processor, the latch to store the performance metric provided by the processor.

However, the reference of Wong does suggest the teaching of a digital tester, which may be a hand-held microprocessor-based controller with a keyboard and a multi-digit display that can be used for network servicing or for low-cost lab-quality engineering setups. (See col. 4, lines 13-16) Furthermore, one skilled in the art would know that latches may be used as storage elements, from which flip-flops are usually constructed. And registers, which are used extensively in the design of digital systems for storing data, consists of a set of flip-flops.

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of testing some PLL dynamic performance parameters. (See col. 6, lines 29-31)

Re claim 34, the combination of Wong further discloses that wherein the RF circuit is integrated onto a first integrated circuit, wherein the processor is integrated onto a second integrated circuit. (In Wong, see fig. 2)

Re claim 35, the reference of Wong fails to explicitly teach that wherein the first and the second integrated circuit are the same integrated circuit.

However, the reference of Wong does suggest the teaching of a IO controller integrated within the same integrated circuit as the RF circuit. (See fig. 2: 22 & 25)

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of minimizing the time delay.

Re claim 36, the combination of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector. (In Wong, see fig. 2)

Re claim 37, the combination of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to a filtered output of a phase detector. (In Wong, see fig. 2: 24 & col. 3, lines 19-22, 50-56)

Re claim 38, the combination of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector and a filtered output of a phase detector. (In Wong, see fig. 2 & col. 3, lines 50-55)

Re claim 39, the combination of Wong further discloses that wherein the circuit permits the testing of the RF circuit in wafer, in packaged integrated circuit, in factory, and in field. (In Wong, see col. 1, lines 38-41, 48-51 & col. 4, lines 16-27)

Re claim 40, the combination of Wong further discloses that wherein the circuit permits the testing of the RF circuit, and wherein the testing is of a type selected from a group consisting of a phase trajectory error, a frequency lock, a frequency deviation, a

phase noise power, or combinations thereof. (In Wong, see fig. 2, 4b & 4c & col. 4, line 34 – col. 6, line 35 & table 2)

2. Claims (48-50, 52-54) are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (hereinafter Kim) (US Patent 6,885,700 B1) in view of Ortiz Perez et al (hereinafter Perez) (US Patent 5,966,428) for the same reasons as set forth in the last office action.

Re claim 48, Kim discloses a method for operating a cellular phone, comprising: performing built-in self-test (BIST) on a parameter associated with the cellular phone. (See col. 6, lines 9-49 "PLL")

But the reference of Kim fails to teach reporting to a cellular service provider through a wireless medium when the BIST reports the parameter to be degraded beyond a limit.

However, Perez does. (See abstract & col. 5, line 26 – col. 6, line 15) Perez discloses a self-diagnostic system for checking all functions of a cellular-transceiver, and reporting the results to an off-site monitoring center by means of the cellular network.

Taking the combined teachings of Kim and Perez as a whole, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, in the manner as claimed and as taught by Perez, for the benefit of reporting the results to an off-site monitoring center.

Re claim 49, the combination of Kim and Perez fails to explicitly teach that wherein the performing step is done on power-up of the cellular phone.

However, the reference of Perez does teach that the system for checking all the functions of the cellular is a self-diagnostic system. (See abstract) Furthermore, it also teaches that it is an auto-diagnostic system. One skilled in the art would know that auto-diagnostic system operate at power-up of the cellular phone to assure that the tranceiver is working properly.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed, for the benefit of checking if the cellular phone is working properly.

Re claim 50, the combination of Kim and Perez further discloses that wherein the parameter is an RF system parameter. (In Kim, see col. 6, lines 9-49 "PLL")

Re claim 52, the combination of Kim and Perez fails to explicitly teach that a step of notifying a user of the cellular phone that the parameter is degraded beyond a limit.

However, the reference of Perez does teach a self-diagnostic system for checking all functions of a cellular-transceiver, and reporting the results to an off-site monitoring center by means of the cellular network in order to check if the tranceiver is working properly.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as

claimed, for the benefit of checking if the cellular phone is working properly.

Re claim 53, the combination of Kim and Perez further discloses that wherein the notifying step is done wirelessly. (In Perez, see abstract "cellular network")

Re claim 54, the combination of Kim and Perez fails to explicitly teach that wherein the notifying step is done through a service bill.

However, the reference of Perez does teach notifying the results to an off-site monitoring center by means of the cellular network. One skilled in the art would know that service bill can also be broadcast wirelessly.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed, for the benefit of optimizing the communication system.

3. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (hereinafter Kim) (US Patent 6,885,700 B1) and Ortiz Perez et al. (hereinafter Perez) (US Patent 5,966,428), as applied to claim 48 above, and further in view of Reddy et al (hereinafter Reddy) (US Patent 6,636,979 B1) for the same reasons as set forth in the last office action.

Re claim 51, the combination of Kim and Perez fails to explicitly teach that wherein the RF system parameter is a distortion in a phase error trajectory.

However, Reddy does. (See col. 5, lines 58-65) Reddy discloses a phase error

measurement circuit used to measure the phase error between two clocks. The circuit can be used as part of a built-in self test (BIST) function to estimate phase error in a PLL.

Taking the combined teachings of Kim, Perez, and Reddy as a whole, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed and as taught by Reddy, for the benefit of detecting the phase error.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) in view of Yamaguchi et al (hereinafter Yamaguchi) (US Patent 6,687,629 B1) for the same reasons as set forth in the last office action.

Re claim 1, Staszewski discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit. (See fig. 4A: "PHE")

But the reference of Staszewski fails to explicitly teach that wherein the signal has a high degree of correlation with an RF output of the RF circuit.

However, one skilled in the art would know that if the loop filter is designed in such as way (adjusting filter's parameters) so that the frequency of the error signal is within the cutoff frequency of the loop filter, then a high degree of correlation can be achieved between the error signal and the output signal.

Therefore, it would have been obvious to one of ordinary skills in the art to

incorporate this feature into the system of Staszewski, in the manner as claimed, for the benefit of achieving synchronization.

The reference of Staszewski discloses the limitations as claimed, except he fails to explicitly teach that wherein the observing occurs outside of the RF circuit; manipulating the signal outside of the RF circuit; and producing a metric for the test outside of the RF circuit based on results from the manipulating.

However, Yamaguchi does. (See fig. 29) Yamaguchi discloses a spectrum analyzer connected to the output of a phase detector, and located outside an RF circuit and a PLL. One skilled in the art would know that the spectrum analyzer (signal analyzer) is capable of observing, manipulating, and generating performance metrics. Furthermore, the concept of measuring and observing the phase detector output outside of a PLL is taught by the reference of Yamaguchi. (See fig. 29) Subsequently, one skilled in the art would have founded obvious to connect a spectrum analyzer to a PLL in order to measure and observe the output of the phase detector, as taught by Yamaguchi.

Taking the combined teachings of Staszewski and Yamaguchi as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, in the manner as claimed and as taught by Yamaguchi, for the benefit of optimizing the performance of the PLL.

Allowable Subject Matter

5. Claims (10 & 44) are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON FLORES whose telephone number is (571)270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. F./
Examiner, Art Unit 2611
December 18, 2008

/David C. Payne/
Supervisory Patent Examiner, Art Unit 2611